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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,599	08/30/2001	Gary L. Swoboda	TI-30481	2479

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EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,599	SWOBODA ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 have been presented for examination based on the application 09/943599 filed on 30 August 2001.

Priority

2. This application appears to be a division of Application No. 09798561, filed 2nd March 2001. A later application for a distinct or independent invention, carved out of a pending application and disclosing and claiming only subject matter disclosed in an earlier or parent application is known as a divisional application or "division." The divisional application should set forth the portion of the earlier disclosure that is germane to the invention as claimed in the divisional application. Application No. 09798561 further claims priority from provisional Applications No. 60186326 & 60219340, filed on the 2nd March 2000.

Information Disclosure Statement

3. An initialed and dated copy of Applicant's IDS form 1449 is attached to the instant Office action.

Specification

4. This instant application does not contain a summary of invention. Appropriate corrections are required.

Claim Interpretation

5. Claim 1 is interpreted to contain only one trace stream with synchronization markers.

Claim Objections

6. Claim 8 recites the limitation "said further synchronization market" in page 43 Line 16 of the claims. There is insufficient antecedent basis for this limitation in the claim. Claim 8 depends from claim 7, which in turn depends from claim 5. There is no antecedent basis for "further synchronization marker", although claim 5 discloses "the synchronization marker". Claim 6 discloses a "further synchronization marker" but is not the parent claim of claim 8. Hence examiner is unclear which synchronization marker the applicants are referring to.

   Examiner respectfully suggests either correcting the language to read, "said synchronization marker" or make claim 8 dependent on claim 6.

7. Claim 11 is objected in light of the claim interpretation presented above for claim 1. Claim 1 is reading on only one stream and claim 11 discloses combining the two streams, hence the objection. Further, it known in the art to combine two streams to make a composite stream.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 discloses:

> "A method of providing data processor emulation information, comprising:
> (a) providing a *program counter trace stream* of program counter values used by a data processor',
> (b) Inserting a synchronization marker into the program counter trace stream; and
> (c) providing trace information indicative of a *data processing operation* performed by the data processor, including identifying a program counter value that corresponds to the data processing operation, said identifying step including expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream."

It is not clear from the claim what is meant by "data processing operation" and how the "trace indicative of data processing operation" is different from the "program counter trace". The specification discloses "data processing operation" (on Pg.8, Line 6) but fails to detail any information about what this trace constitutes and any need for a separate trace.

Claims 2-12 are rejected for incorporating the deficiencies of claim 1 by dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claim 1-10 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No 6,009,270 issued to Daniel Mann (Mann '270 hereafter).

Regarding Claim 1

Mann '270 teaches:

> "A method of providing data processor emulation information, comprising:
> providing a *program counter trace stream* of program counter values used by a data processor;"

as a trace stream (Mann '270: Col.14, Lines 48-50) containing address information for reconstructing instruction execution flow (Mann '270: Col. 2, Lines 60-64). It is known in the art that program counter contains op-code and address information for the operands for each instruction. A stream of program counter will provide an instruction flow in a program counter. Hence the stream taught by Mann '270 is equivalent to program counter trace stream.

Mann '270 also teaches:

> "Inserting a synchronization marker into the program counter trace stream; and"

as insertion of a synchronizing address information (current program address) to synchronize trace based on the state of synchronization register (TSYNCH) (Mann '270: Col.16, Lines 3-5; Col.16, Lines 25-29).

Teachings of Mann '270 are applied to claim 1 as understood from ***Claim Interpretation*** section above.

Mann '270 also teaches:

> "providing trace information indicative of a *data processing operation* performed by the data processor, including identifying a program counter value that corresponds to the data processing operation, said identifying step including expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream."

As one stream trace containing program execution information including synchronization markers (Mann '270: Abstract Lines1-4) performing data processing and I/O operations (Mann '270: Col.10, Lines 9-11). Mann further teaches that branching causes disruption in the flow and non-data dependent branching (where new address is not dependent on address in data registers) (Mann '270: Col.13, Lines 56-62) can be represented in a form of an offset indicating whether the branch was taken or not. This offset information is presented in form of a trace entry (Mann '270: Col.14, Lines 7-16) from which new target value can be reconstructed (Mann '270: Col. 15 Lines 8-13, 53-56).

Regarding Claim 2

Mann '270 teaches that branching causes disruption in the program flow and new target addresses need to be accessed may be in memory location (Mann '270: Col. 13, Lines 59-62). Hence the processor may perform a memory access operation.

Regarding Claim 3

Mann '270 teaches that the data processor detects the program counter load present in the each trace record (Mann '270: Col.16, Lines 13-15).

Regarding Claim 4

Mann '270 teaches that the counter counts the program counter loads (Mann '270: Col.16, Lines 35-44; Figure 7).

Regarding Claim 5

Mann '270 teaches counter keeps a running count of program counter loads since the insertion of program counter (Mann '270: Col.16, Lines 25-29, Lines 48-53), thereby resetting the counter whenever the synchronization happens (Mann '270: Col.16, Lines 45-47).

Regarding Claim 6

Mann '270 teaches resetting the counter to a predetermined value (Mann '270: Col.16, Lines 16-21) as set in the TSYNCH register, in response to the insertion of synchronization.

Regarding Claim 7

Mann '270 teaches updating the counter in response to the program counter loads as disclosed in claim 4 for the disclosed maintaining step. Mann '270 also teaches the updating step as equating counter values to the offset. This offset defines what would be the next program counter values based on which conditional branch was taken (Mann '270: Col.13, Line 67; Col.14 Lines: 1, 7-16). Based on that information

next address can be computed (Mann '270: Col.15, Lines 7-11) and there is no need to provide complete address information (Mann '270: Col.15, Lines 61-67).

Regarding Claim 8

Claim 8 is rejected for the same reason as claim 6 as it claims the same limitations.

Regarding Claim 9

Mann '270 teaches that insertion of offset in claim 1 and inserting the offset in further trace stream is just insertion of subsequent trace containing the offset. It is inherent to the trace stream design that subsequent trace entries may also contain an offset for branch statements. Mann '270 does not provide any limitation that above-mentioned functionality cannot be part of his design.

Regarding Claim 10

Claim 10 is rejected for the same reason as claim 9 as it claims the same limitations. Claim 9 & 10 are both dependent claims from claim 1, which defines the offset.

Regarding Claim 12

Mann '270 discloses that program counter may need to provide address information where address is data dependent (Mann '270: Col.15, Lines 66-67;Col.16, Lines 1-2) and simple branch tracing cannot be provided. Hence providing the complete program counter entry.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 13-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,764,885 issued to Richard L. Sites et al (Sites '885 hereafter) in view of U.S. Patent No. 6,009,270 issued to Daniel Mann (Mann '270 hereafter).

Regarding Claim 13

Sites '885 teaches:

> An apparatus for providing data processor emulation information, comprising:
> first and second inputs for coupling to a data processor;

as an apparatus containing a data processor (Sites '885: Figure 1C, Element 139) having two inputs each representing data stream from instruction cache (Sites '885: Figure 1C, Element 137) and data cache (Sites '885: Figure 1C, Element 138).

Sites '885 also teaches:

> a trace stream generator coupled to said first input for providing a program counter trace stream of program counter values used by the data processor, said trace stream generator operable for inserting a synchronization marker into the program counter trace stream;

as a trace stream generator (Sites '885: Figure 1C, Element 150, I Trace Logic) coupled to first input providing a program counter trace stream (Sites '885: Figure 1C, Element 101) through the aforementioned data processor. I Trace Logic described by Sites '885 also inserts the synchronization markers in the trace stream entries (Sites '885: Figure 2, Elements 210,220& 230) as time indices (Sites '885: Figure 2, Element 202; Col.5, Lines 61-67).

Sites '885 also teaches:

> and a trace apparatus coupled to said second input for providing trace information indicative of a data processing operation performed by the data processor, including a program counter identifier for identifying a program counter value that corresponds to said data processing operation, said program counter identifier operable for expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program

counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream.

As a trace apparatus mapped to D Trace Logic (Sites '885: Figure 1C, Element 160) connected to second input indicative of data processing operation, concerning data, coming from D Cache (Sites '885: Figure 1C, Element 135). Sites also teaches how function of the program counter identifier can implemented to create program counter values for direct program counter loads (Sites '885: Col.9, Lines 60-67) and conditional branching (Sites '885: Col.9, Lines 1-14). Further, Sites '885 teaches creating a synchronization marker in the second stream, wherein the synchronization marker is in the form of time stamp (Sites '885: Col.5, Lines 61-67; Figure 2, Element 202) in a data processing entry (Sites '885: Figure 2, Element 270).

Sites '885 do not teach creating a program counter offset based on the synchronization marker in the same stream.

Mann '270 above teaches using a synchronization marker (Mann '270: Col.16, Lines 3-5; Col.16, Lines 25-29). Further, This offset information is presented in form of a trace entry (Mann '270: Col.14, Lines 7-16) from which new target value can be reconstructed (Mann '270: Col. 15 Lines 8-13, 53-56).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to take Mann '270's teachings and apply them to Sites '885 design of using separate streams for program counter and data processing operations. The motivation would be that such synchronization would provide address information frequently enough for reconstructing instruction

execution flow with offset in second stream, making a tighter coupling between the two streams. Time indices used in the Sites '885 reference provide good idea what a target PC value was currently used, looking at the stream history (Sites '885: Figure 2) but may not be provided frequently enough. Mann's concept of counter based synchronization overcomes such a loss of reference to tie two streams together.

Regarding Claim 14

Mann '270 teaches that the data processor detects the program counter load present in the each trace record (Mann '270: Col.16, Lines 13-15).

Regarding Claim 15

Mann '270 teaches that the counter counts the program counter loads (Mann '270: Col.16, Lines 35-44; Figure 7).

Regarding Claim 16

Mann '270 teaches counter keeps a running count of program counter loads since the insertion of program counter (Mann '270: Col.16, Lines 25-29, Lines 48-53), thereby resetting the counter whenever the synchronization happens (Mann '270: Col.16, Lines 45-47).

Regarding Claim 17

Mann '270 teaches resetting the counter to a predetermined value (Mann '270: Col.16, Lines 16-21) as set in the TSYNCH register, in response to the insertion of synchronization.

Regarding Claim 18

Mann '270 teaches that insertion of offset in claim 13 and inserting the offset in further trace stream is just insertion of subsequent trace containing the offset. It is inherent to the trace stream design that subsequent trace entries may also contain an offset for branch statements. Mann '270 does not provide any limitation that above-mentioned functionality cannot be part of his design.

Regarding Claim 19

Sites '885 teaches, combining the two streams in Trace Queue (Sites '885: Figure 1C, Element 200) coming from D Trace Logic (equivalent to trace apparatus) and I Trace Logic (equivalent to trace stream generator) and outputting the composite stream in a Trace Driver (Sites '885: Figure 1C, Element 190).

Regarding Claim 20

Mann '270 teaches that branching causes disruption in the program flow and new target addresses need to be accessed may be in memory location (Mann '270: Col. 13, Lines 59-62). Hence the processor may perform a memory access operation.

Regarding Claim 21

Teachings of Mann '270 are disclosed in claim 13. Mann '270 teaches program counter identifier as Counter (Mann '270: Figure 7, Element 701), which gets information that synchronization event (providing complete Program Counter with target address) has happened from Trace Control Circuit (Mann '270: Figure 7, Element 218). This resets the Counter mentioned above (Mann '270: Col.15, Lines 45-47, 35-38).

Regarding Claim 22

Trace stream generator is equivalent to Trace Control in the Mann '270 reference, as Mann uses just one trace stream. It can be clearly seen from Mann reference (Mann '207: Figure 7) that Trace Control (Element 218) is coupled to the Counter (Element 701) and control the Counter.

11. Claim 23-26 ~~is~~ are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,764,885 issued to Richard L. Sites et al (Sites '885 hereafter) in view of U.S. Patent No. 6,009,270 issued to Daniel Mann (Mann '270 hereafter), further in view of U.S. Patent No. 6,732,307 issued to David A. Edwards (Edwards '307 hereafter).

Regarding Claim 23

Sites '885 and Mann '270 teachings' are mentioned above in rejection for claim 13. Sites '885 and Mann '270 teaches an apparatus with same limitations as claim 23 above.

Sites '885 and Mann '270 do no disclose an integrated circuit with the limitations disclosed in claim 13.

Edwards '307 teaches an integrated circuit design which extract and export the trace information from a data processor (Edwards '307: Figure 1), hence performing the same function and being is analogous art to Sites '885 and Mann '270.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to take teachings of Edwards '307 and apply them to Sites '885 and Mann '270. The motivation would have been to reduce bandwidth for off-chip trace transmission to an external system by providing on-chip trace handling and compression (Edwards '307: Col.1, Lines 13; Col.2 Lines 41-44).

Regarding Claim 24

Sites '885 and Mann '270 teachings are disclosed in rejection for claim13. Sites '885 and Mann '270 teach an apparatus with same limitations as claim 24 above.

Mann '270 also teaches an emulation controller to load the instructions that need to be executed on the target data processor (Mann '270: Col.4, Lines 10-13 & Figure 1; Col.4, Lines 55-57 & Figure 2).

Sites '885 and Mann '270 do no disclose an integrated circuit system with the limitations disclosed above.

Edwards '307 teaches an integrated circuit system (Edwards '307: Figure 1) containing a debug circuit (Edwards '307: Figure 2, Element 103 - emulation controller) as well, performing the same function as disclosed by Sites '885 and Mann '270.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to take teachings of Edwards '307 and apply them to Sites '885 and Mann '270. The motivation would have been to reduce bandwidth for off-chip trace transmission to an external system by providing on-chip trace handling and compression (Edwards '307: Col.1, Lines 13; Col.2 Lines 41-44). Further motivation comes from the fact that system-on-chip (SOC) concept is well known in the art with its benefits to reduce intersystem delays and speed up communication among systems on the chip. In our present invention debug circuit system interfaces with the data processor and is a part of SOC (Edwards '307: Figure 1).

Regarding Claim 25 & 26

Teachings of Edwards are disclosed above in claims 27. Edwards also teaches that the debug system (emulation controller) is connected to external system (Edwards: Col.6, Lines 12-14). An external system could be a host computer running the debug tool mentioned by Edwards (Edwards: Col 7, Lines 46-48). A keyboard constitutes a "tactile interface" and a computer monitor constitutes a "visual interface". Official notice is taken that it is well known in the art to use a keyboard and a computer monitor with a computer (host interface) to form a man-machine interface.

Remarks

All claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

as

JEAN R. HOMERE
PRIMARY EXAMINER